

CLAIMS

What is claimed:

1 1. A method for forming a semiconductor device comprising:
2 forming a 3-dimensional (3D) pattern in a substrate; and
3 depositing at least one material over the substrate in accordance with desired
4 characteristics of the semiconductor device.

1 2. The method of claim 1 wherein forming the 3D pattern further comprises:
2 depositing a layer of material onto the substrate;
3 imprinting a 3D pattern into the layer of material; and
4 transferring the 3D pattern into the substrate.

1 3. The method of claim 1 wherein the semiconductor device comprises a cross-point
2 memory array.

1 4. The method of claim 2 wherein the semiconductor device is at least one of a
2 transistor, a resistor, a capacitor, a diode, a fuse and an anti-fuse.

1 5. The method of claim 2 wherein imprinting a 3D pattern into the layer of material
2 further comprises utilizing a 3D stamping tool to create the 3D pattern.

1 6. The method of claim 2 wherein imprinting a 3D pattern into the layer of material
2 further comprises utilizing a molding process to imprint the 3D pattern into the layer of
3 material.

1 7. The method of claim 2 wherein the layer of material comprises a polymer
2 material.

1 8. The method of claim 2 wherein the layer of material comprises a photo-resist
2 material.

1 9. The method of claim 2 wherein transferring the 3D pattern into the substrate
2 includes:

3 removing a portion of the layer of material thereby exposing a portion of the
4 substrate;

5 etching the exposed portion of the substrate;

6 removing another portion of the layer of material thereby exposing a second
7 portion of the substrate;

8 etching the second portion of the substrate; and

9 removing a remaining portion of the layer of material.

1 10. The method of claim 3 wherein depositing at least one material over the substrate
2 further comprises:

3 depositing two sets of conductors with a semiconductor layer there between to form
4 row and column electrodes overlaid in such a manner that each of the row electrodes
5 intersects each of the column electrodes at exactly one place.

1 11. The method of claim 9 wherein depositing at least one material over the substrate
2 further comprises:

3 depositing a first metal layer on the substrate;
4 applying a first planarizing polymer to the metal layer;
5 removing a portion of the first planarizing polymer;
6 utilizing the first planarizing polymer as an etch mask to etch the first metal layer
7 thereby leaving a remaining portion of the first metal layer;
8 etching the substrate in a selective fashion; and
9 removing the first planarizing polymer.

1 12. The method of claim 11 wherein depositing at least one material over the
2 substrate further comprises:

3 depositing a second metal layer on the remaining portion of the first metal layer;
4 applying a second planarizing polymer to the second metal layer;
5 removing a portion of the second planarizing polymer;
6 utilizing the second planarizing polymer as an etch mask to etch the second metal
7 layer; and
8 removing the second planarizing polymer.

1 13. A system for forming a semiconductor device comprising:
2 means for forming a pattern in a substrate wherein the pattern is 3-dimensional;
3 and
4 means for depositing at least one semiconductor material over the substrate in
5 accordance with desired characteristics of the semiconductor device.

1 14. The system of claim 13 wherein the semiconductor device comprises a cross-point

2 memory array.

1 15. The system of claim 13 wherein the means for forming the pattern further
2 comprises:

3 means for depositing a layer of material onto the substrate;
4 means for imprinting a 3D pattern onto the layer of material; and
5 means for transferring the 3D pattern into the substrate.

1 16. The system of claim 14 wherein the means for depositing at least one
2 semiconductor material over the substrate further comprises:

3 means for depositing two sets of conductors with a semiconductor layer there
4 between to form row and column electrodes overlaid in such a manner that each of the row
5 electrodes intersects each of the column electrodes at exactly one place.

1 17. The system of claim 14 wherein the semiconductor device is at least one of a
2 transistor, a resistor, a capacitor, a diode, a fuse and an anti-fuse.

1 18. The system of claim 15 wherein the means for imprinting a 3D pattern into the layer
2 of material further comprises means for implementing a molding process to imprint the 3D
3 pattern into the layer of material.

1 19. The system of claim 15 wherein the means for transferring the 3D pattern into the
2 substrate includes:

3 means for removing a portion of the layer of material thereby exposing a portion

4 of the substrate;

5 means for etching the exposed portion of the substrate;

6 means for removing another portion of the layer of material thereby exposing a
7 second portion of the substrate;

8 means for etching the second portion of the substrate; and

9 means for removing a remaining portion of the layer of material.

1 20. The system of claim 15 wherein the means for imprinting a 3D pattern onto the
2 layer of material further comprises means for utilizing a 3D stamping tool to create the 3D
3 pattern.

1 21. The system of claim 15 wherein the means for depositing at least one
2 semiconductor material over the substrate further comprises:

3 means for depositing a first metal layer;

4 means for applying a planarizing polymer to the first metal layer;

5 means for removing a portion of the planarizing polymer;

6 means for utilizing the planarizing polymer as an etch mask to etch the first metal
7 layer thereby leaving a remaining portion of the first metal layer;

8 means for etching the substrate in a selective fashion; and

9 means for removing the planarizing polymer.

1 22. The system of claim 15 wherein the layer of material comprises a polymer
2 material.

1 23. The system of claim 15 wherein the layer of material comprises a photo-resist
2 material.

1 24. The system of claim 21 wherein the means for depositing at least one
2 semiconductor material over the substrate further comprises:

3 means for depositing a second metal layer on the remaining portion of the first
4 metal layer;

5 means for applying a second planarizing polymer to the second metal layer;

6 means for removing a portion of the second planarizing polymer;

7 means for utilizing the second planarizing polymer as an etch mask to etch the
8 second metal layer; and

9 means for removing the second planarizing polymer.

1 25. A method for forming a semiconductor device comprising:

2 forming a 3-dimensional (3D) pattern in a substrate;

3 depositing a first metal layer on the substrate;

4 applying a first planarizing polymer to the metal layer;

5 removing a portion of the first planarizing polymer;

6 utilizing the first planarizing polymer as an etch mask to etch the first metal layer

7 thereby leaving a remaining portion of the first metal layer;

8 etching the substrate in a selective fashion; and

9 removing the first planarizing polymer.

1 26. The method of claim 25 wherein the semiconductor device comprises a cross-

2 point memory array.

1 27. The method of claim 25 further comprising:

2 depositing a second metal layer on the remaining portion of the first metal layer;

3 applying a second planarizing polymer to the second metal layer;

4 removing a portion of the second planarizing polymer;

5 utilizing the second planarizing polymer as an etch mask to etch the second metal

6 layer; and

7 removing the second planarizing polymer.

1 28. A semiconductor device comprising:

2 a substrate wherein the substrate comprises a 3D pattern formed therein;

3 at least one material deposited thereon in accordance with desired characteristics

4 of the semiconductor device.

1 29. The semiconductor device of claim 28 wherein the 3D pattern is formed with the

2 following process:

3 depositing a layer of material onto the substrate;

4 imprinting a 3D pattern into the layer of material; and

5 transferring the 3D pattern into the substrate.

1 30. The semiconductor device of claim 29 wherein transferring the 3D pattern into the

2 substrate includes:

3 removing a portion of the layer of material thereby exposing a portion of the

4 substrate;

5 etching the exposed portion of the substrate;

6 removing another portion of the layer of material thereby exposing a second

7 portion of the substrate;

8 etching the second portion of the substrate; and

9 removing a remaining portion of the layer of material.